REMARKS

Claims 1-3, 6 and 8-11 are pending. Claim 1 has been amended. The Applicants respectfully request reconsideration of these Claims based on the remarks that follow.

103 Rejection

Claims 1-3, 6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horden et al. (5,812,860) in view of Weiss et al. (5,774,703). The Applicants have reviewed the cited references and respectfully submit that the present invention as recited in Claims 1-3, 6 and 8-11 is neither shown nor suggested by Horden et al. (5,812,860) and Weiss et al. (5,774,703) either alone or in combination.

The Examiner is respectfully directed to independent Claim 1 which recites that an embodiment of the present invention is directed to a method for controlling the operating condition of a computer processor on a chip, comprising:

> ... dynamically changing the operating condition of the processor by changing one of the frequencies generated by the clock generator and the voltage to the maximum frequency and the minimum voltage determined, wherein a plurality of clock frequencies are provided which can be individually selected concurrently.

Independent Claims 2, 6, and 8 recite limitations similar to those found in independent Claim 1. Claim 3 depends from independent Claim 2, and Claims 9-11 depend from independent Claim 8. These Claims recite further features of the presently claimed invention.

Horden et al. does not anticipate or render obvious a method for controlling the operating condition of a computer processor on a chip that wherein "a plurality of clock frequencies are provided which can be individually selected concurrently" as claimed. The Horden et al. reference discloses a data processing system that has the capacity to provide multiple voltages and frequencies to a core processor 1 (see Figure 1). It should be appreciated that the Horden et al. reference teaches that the multiple voltages and frequencies that are provided to core processor 1 and its peripherals 17 (see Figure 1) are provided over a period of time and are based on the real time criteria that is extant at given points during that period of time. However, it is important to note that in contrast to the system that is set forth in Applicants Claims 1, 2, 6, and 8, in the system disclosed by Horden et al., at any given point in time the same voltage and frequency that is provided to core processor 1 is also provided to all of the peripheral components 17 of the core processor (see column 3, lines 1-5). Consequently, a plurality of voltages and frequencies are not provided concurrently (because in the Horden et al. system the same voltages and frequencies are provided concurrently) in the system of Horden et al. as is required to meet the limitations that are set forth in the Applicants' independent Claims 1, 2, 6 and 8.

By contrast, Applicants' independent Claims 1, 2, 6, and 8 set forth a method whereby more than one frequency may be generated by a clock generator and whereby each of the generated frequencies may be selected and provided concurrently (e.g., such as to different components of the recited computer processor and at the same point in time). Nowhere in the Horden et al. reference is such a feature taught or suggested. In fact, the Horden et al. reference actually ***teaches away*** from the incorporation of such a feature as a component of it's disclosed systems design. This is because the incorporation

of this feature would undermine an essential principle of the Horden et al. systems operation. In contrast to the system set forth in the Applicant's Claims, the operation of the data processing system disclosed by the Horden et al. reference is based on the concurrent distribution of the same voltages and frequencies that are supplied to a core processor 1 of the disclosed system to peripheral components 17 of the core processor. Consequently, Horden et al. does not show or suggest the Applicants' invention as it is set forth in Claims 1, 2, 6, and 8.

The cited combination fails to teach or suggest the claimed embodiment. Moreover, Weiss et al. does not overcome the shortcomings of Horden et al. noted above. It has been held that the teachings of a reference are not sufficient to render an invention obvious where the "suggested combination of references would require a substantial reconstruction and redesign of the elements shown in the primary reference as well as a change in the basic principle under which the construction was designed to operate." *In re Ratti*, 270 F.2d. 810, 123 USPQ 349 (CCPA). The Weiss et al. reference discloses a data processing system that includes registers whose supplied clock speed (e.g., frequency) may be controlled independently of a clock speed supplied to a core processor of the system. The Examiner alleges that it would have been obvious to provide the system disclosed by Horden et al. with a clock distribution scheme such as is disclosed in the Weiss et al. reference "as it would have made it easier to optimize different subsystems of the processor ..." (see Office Action page 3). However, to impose a clock distribution scheme such as is disclosed in the Weiss et al. reference on the system disclosed by Horden et al. would change a basic principle under which the construction of the system disclosed by the Horden et al. reference was designed to operate since, as

previously mentioned, the operation of that system is based on the concurrent distribution of the same voltages and frequencies that are supplied to core processor 1 of the system to peripheral components 17 (see Figure 1) of the core processor. Neither reference suggests such a combination. Consequently, Horden et al. and Weiss et al. either alone or in combination do not anticipate or render obvious the Applicants' claimed invention as set forth in Claims 1, 2, 6, and 8.

Therefore, Applicants respectfully submit that Horden et al. and Weiss et al. either alone or in combination do not anticipate or render obvious the present claimed invention as is recited in Claims 1, 2, 6 and 8 and, as such, Claims 1, 2, 6, and 8 traverse the Examiner's basis for rejection under 35 U.S.C. §103. Accordingly, Applicants respectfully submit that Claims 1, 2, 6, and 8 are in condition for allowance. In addition, the Applicants respectfully submit that Horden et al. and Weiss et al. either alone or in combination do not anticipate or suggest the present invention as is recited in Claim 3 dependent on Claim 2, and Claims 9-11 dependent on Claim 8, and that these Claims are also in condition for allowance as being dependent on allowable base claims.

SUMMARY

In view of the foregoing amendments and remarks, Applicants respectfully submit that the pending claims are in condition for allowance. Applicants respectfully request reconsideration of the application and allowance of the pending claims.

MARKED-UP VERSION TO SHOW CHANGES

1. A method for controlling the operating condition of a computer processor on a chip [including a clock generator on the chip capable of providing a plurality of clock frequencies which can be individually selected concurrently] comprising the steps of:

determining a maximum allowable power consumption level from the operating condition of the processor,

determining a maximum frequency which provides

power not greater than the allowable power consumption level,

determining a minimum voltage which allows operation at the maximum frequency determined, and

dynamically changing the operating condition of the processor by

changing one of the frequencies generated by the clock generator and the voltage to the maximum frequency and the minimum voltage determined, wherein a plurality of clock frequencies are provided which can be individually selected concurrently.